John Alsop

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RESEARCH INTERESTS

My recent research has focused on the challenges that arise when specializing data movement (coherence, consistency, near-memory computing) in emerging heterogeneous systems. More generally, I'm interested in computer architecture, heterogeneous computing, emerging memory systems, and the hardware-software interface.

EDUCATION

University of Wisconsin-Madison   (Sep 2007 - Dec 2011)   GPA 3.84/4.0
B.S. Computer Engineering, Computer Science

Technical University of Munich   (Oct 2009 - Aug 2010)
Exchange Student: Electrical and Computer Engineering

University of Illinois at Urbana-Champaign   (Sep 2013 - present)   GPA 3.97/4.0
PhD Candidate: Electrical and Computer Engineering

ACADEMIC EXPERIENCE

Research Assistant with Prof. Sarita Adve, UIUC   (Jan 2014 – August 2018)
- *Spandex: A flexible coherence interface for heterogeneous devices with diverse memory demands and coherence strategies [ISCA'18].*
- *Heterogeneous relaxed atomics project: defining semantics and evaluating the performance impact of relaxed atomics in a CPU-GPU system [ISCA'17]*
- *GPU stall profiling project: identifying sources of GPU stalls in a CPU-GPU system [ISPASS'16]*
- *GPU smart scheduling project: scheduling GPU thread blocks to maximize locality*
- *DeNovo for GPU project: achieving efficient synchronization in GPUs without the need for scopes [MICRO'15]*
- *Stash project: combining the benefits of GPU scratchpad and cache in one specialized memory [ISCA'15]*

Teaching Assistant, University of Illinois   (Sep 2013 - Dec 2013)
- *Supervised and assisted undergraduate students in ECE385: Digital Systems Laboratory*
- *Evaluated lab projects and coursework*
- *Earned **Outstanding Teaching Assistant** award*

AWARDS AND SIGNIFICANT RECOGNITION

- Rambus Computer Engineering Fellowship 2017
- Dan Vivoli Endowed Fellowship 2016
- Stash work [ISCA'15] selected as an IEEE Micro Top Picks 2016 Honorable Mention.
- GPU consistency work [MICRO'15] selected as an IEEE Micro Top Picks 2016 Honorable Mention
- Stash work [ISCA'15] featured in Computing Community Consortium (CCC) blog: http://www.cccblog.org/2015/09/08/cache-or-scratchpad-why-choose/
- Fall 2013 Outstanding Teaching Assistant (top 10% of TAs based on student evaluations)
- Graduate with distinction from the University of Wisconsin
- Richardson Engineering Scholarship 2009

PUBLICATIONS

- M. Huzaifa, **J. Alsop**, A. Mahmoud, G. Salvador, M. D. Sinclair, and S. V. Adve, "Inter-kernel Reuse-aware Thread Block Scheduling." In *Transactions on Architecture and Code Optimization,* 2020.

- G. Salvador, W. H. Darvin, M. Huzaifa, **J. Alsop**, M. D. Sinclair, and S. V. Adve, "Specializing Coherence, Consistency, and Push/Pull for GPU Graph Analytics." *arXiv preprint arXiv:2002.10245 (2020)*.

- **J. Alsop**, M. D. Sinclair, S. Bharadwaj, A. Dutu, A. Gutierrez, O. Kayiran, M. LeBeane, S. Puthoor, X. Zhang, T. Tai Yeh, B. M. Beckmann, "Optimizing GPU Cache Policies for MI Workloads." *IEEE International Symposium on Workload Characterization,* 2020.

- **J. Alsop**, M. D. Sinclair, and S. V. Adve, "Spandex: A Generalized Interface for Flexible Heterogeneous Coherence." In *International Symposium on Computer Architecture,* 2018.

- M. D. Sinclair, **J. Alsop**, and S. V. Adve, "HeteroSync: A Benchmark Suite for Fine-Grained Synchronization on Tightly Coupled GPUs." in *IEEE International Symposium on Workload Characterization (IISWC)*, 2017.

- M. D. Sinclair, **J. Alsop**, and S. V. Adve, "Chasing away RAts: Semantics and evaluation for relaxed atomics on heterogeneous systems," in *International Symposium on Computer Architecture,* 2017.

- **J. Alsop**, M. Orr, B. Beckmann, D. Wood, "Lazy release consistency for GPUs," in *49th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, IEEE, 2016.

- **J. Alsop**, M. D. Sinclair, R. Komuravelli, and S. V. Adve, "Characterizing the sources of memory stalls for tightly coupled GPUs," in *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, IEEE, 2016.

- M. D. Sinclair, **J. Alsop**, and S. V. Adve, "Efficient GPU synchronization without scopes: Saying no to complex consistency models," in *48th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, IEEE, 2015. **IEEE Micro Top Picks 2016 Honorable Mention**

- R. Komuravelli, M. D. Sinclair, **J. Alsop**, M. Huzaifa, M. Kotsifakou, P. Srivastava, S. V. Adve, and V. S. Adve, "Stash: Have your scratchpad and cache it too," in *Proceedings of the 42nd Annual International Symposium on Computer Architecture (ISCA)*, pp. 707–719, ACM, 2015. **IEEE Micro Top Picks 2016 Honorable Mention**, featured in **Computing Community Consortium** (CCC) blog

INDUSTRY EXPERIENCE

AMD Research – Bellevue, WA
Senior Design Engineer   (Oct 2018 - present)
Researching ways to improve performance and power efficiency in future heterogeneous memory systems.

AMD Research – Bellevue, WA
Co-op Engineer   (Jun 2015 - Apr 2016)
Investigated ways to improve coherence and consistency in tightly coupled CPU-GPU systems in order to enable efficient fine-grained synchronization [MICRO'16]. Contributed to GEM5 and the AMD GPU architectural simulator.

ADDITIONAL SKILLS

C[++], Python, shell, Java, Verilog, VHDL, PHP/HTML/CSS, SQL, gem5, GPGPU-Sim, git, svn, vim